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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,070	11/20/2003	Hendrik F. Hamann	YOR920030368US1 (8728-643	8659

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EXAMINER	
GEORGE, PATRICIA ANN	
ART UNIT	PAPER NUMBER
1765	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/718,070	HAMANN ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-13,22,23 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-13,22,23,and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4, 5, 7, 11, 12, 13, 22, 23 and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6,927,410), in view of Lowrey et al (6,943,365) (herein referred to as Lowrey) evidenced by Hun Seo et al. (Investigation of Crystallization Behavior of Sputter-Deposited Nitrogen-Doped Amorphous $Ge_2Sb_2Te_5$ Thin Films; Jpn. J. Appl. Phys. Vol.39 (2000) 745-751; Part 1, No. 2B, 28 February 2000).

Chen teaches: a multi-bit phase changing memory device (ab.), including: layers of phase change material (ab.) separated by layers of conductive interface (ab.), produced with varying degrees of resistivity (col.2, l.27).

Chen teach a multi-bit phase change memory cell (claim1) or multi-bit phase change memory (claim 22), where each of said plurality of phase change material layers has a different height from one another, please refer to: column 1, lines 35 through column 2, lines 36, where Chen teaches phase change memory devices, such as multi-

bit memory cells, i.e. multi-bit phase change memory cell (claim 1) and i.e. multi-bit phase change memory (claim 22); and see column 8, lines 28-36, where Chen teaches a plurality of phase change material layer with different thicknesses, i.e. where plurality of phase change material layers has a different height from one another. The term thickness is interpreted as a dimension between two surfaces, as opposed to length or width, i.e. used to describe the height of a semiconductor layer.

Although Chen describes the thickness of the phase change material layers may be different from one another, Chen is silent to the height increasing while surface area decrease, of each of the phase change materials along a direction from the first outer conductor layer to the second outer conductive layer, as in claim 1.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to select any desired height and surface area, of each of the phase change materials along a direction from the first outer conductor layer to the second outer conductive layer, as in applicants' claimed limitation, when forming the multi-bit phase changing memory device, as Chen, because Chen teaches it is effective to provide phase change material layers of varying thickness that are different from one another. In the absence of unexpected results, one of ordinary skill would form the phase change layers as desires, including applicants' specifically claimed height increasing while surface area decrease, of each of the phase change materials along a direction from the first outer conductor layer to the second outer conductive layer, because the reference does not limit the ordered configuration of phase change materials.

Further, because Chen discloses a plurality of phase change material layers with different thicknesses, see column 8, lines 28-36, one of ordinary skill in the art would recognize that the plurality of phase change material layers with different thicknesses, as in the reference of Chen, would also have different surface areas from one another, because the mathematical equation for surface area is dependent on height (i.e. thickness) as a multiplier, and a variety of heights would calculate a result with a variety of surface areas. Applicants' have not shown anything unexpected when forming the claimed ordered configuration of phase change materials.

Chen does not teach the structure of the first and second conductive layers, disposed on opposite sides of the memory cell, as in claim 1.

Lowrey illustrates the first outer conductive layer (130a) disposed at the right side (i.e. one side) of the memory cell and a second outer conductive layer (130b) disposed at the left side (i.e. a side opposite to the one side) of the memory cell, in figure 1A, and refers to this configuration as the "rapier" design of conductor spacer.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the structure of the first and second conductive layers, disposed on opposite sides of the memory cell, as in Lowrey, when forming the multi-bit phase changing memory device, of Chen, because Lowrey teaches this configuration is an improvement as it reduces the size of the area of contact of the memory material, thereby reducing the total current needed to program the memory device.

As to the limitation wherein each of the plurality of phase change material layers have the same resistivity, Chen teaches phase change memory devices use memory materials that are electrically switched (programmed) between different structured states that exhibit different electrical read-out properties. For example, memory devices are programmed between a generally amorphous state that exhibits a relatively high resistivity, and a generally crystalline state that exhibits a relatively low resistivity. The phase change material is programmed by heating the material, whereby the amplitude and duration of the heating dictates whether the phase change material is left in an amorphous or crystallized state. The high and low resistivities represent programmed bit values of "1" and "0", which can be sensed by then measuring the resistivity of the phase change material, which is written on plurality of phase change material layers have the same resistivity (see background, lines 35-52). Chen further teaches first a high current pulse is passed through the memory device to generate a thermal pulse that amorphousizes *all* of the phase change material layers. Then a crystallizing thermal pulse creates a temperature gradient across the memory material, where the various layers are *asymmetrically* heated (i.e. top layers hotter than bottom layers). Over the duration of the crystallizing thermal pulse, the various layers of phase change materials are sequentially crystallized, top down, one layer at a time, which is also written on plurality of phase change material layers have the same resistivity.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, that the programmed bit vaulues of "1" and "0" represent high and low resistivities, which can be sensed by then measuring the resistivity of the phase

change material; that the step which includes a high current pulse, resets all the phase change material layers, preparing them to be programmed with a thermal pulse; and when the high current pulse resets all the phase change material layers they have the same programming value and the same resistivity.

Further on the same topic, Seo et al. provides evidence that nitrogen doping (i.e. implanting) of the Ge2Sb2Te5 phase-change films allows the crystalline process to occur in a primary nucleation step, an improved stability of the amorphous phase. Seo et fails to explicitly teach implanting the Ge2Sb2Te5 have an effect on the resistivity of the mater, however it would have been obvious to one of ordinary skill in the art at the time of invention was made, that an improvement to the stability of of the amorphous phase of Ge2Sb2Te5 that allows the crystalline process to occur in one primary nucleation step would greatly impact the resistivity of the film because it would allow for a change to the state of the resistance to occur more rapidly and remain fixed in that state until another change is desired, therefor allowing all the phase change material layers to be more responsive to holding the same value of resistivity when programmed as less device failure occurs, clearly an improvement in manufacturing.

As for claim 2, Chen illustrates in figure 6, the ability to set the electrical resistance of each of the plurality of phase change material layers in an increasing manner, sequentially, from layer 1 through later 5, pointing to a direction from the first outer conductive layer to the second outer conductive layer.

As for claim 4, Chen's figures 4A-G illustrate wherein each of the plurality of phase change material layers have a different phase transition temperature, also concealed in column 5, lines 23-26.

As for claim 5, Chen explains a method for operating a phase change memory having a volume of memory material, including a plurality of discrete layers of materials. The method includes applying heat to the volume of material for a predetermined amount of time (col.3, l.28-43), which demonstrates the following limitation claimed: each of the plurality of phase change material layers has the same phase transition temperature.

As for claim 7, in figure 3 (explained in col.4, l. 27-49), Chen illustrates a plurality of conductive layers (fig. 3, 26/24/28), including a plurality of intermediate layers (fig.3, 24), disposed between the first (fig.3, 26) and second (fig. 3, 28) outer conductive layers, each of the intermediate conductive layers (fig.3, 24) having the same dimensions as an adjacent phase change material layer.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to

Although the reference of Chen teaches intermediate conductive layers has a greater height and greater thickness than the height and thicknesses of each of the phase change material layers, it would have been obvious to one of ordinary skill in the art at the time of invention was made, that the intermediate conductive layers have the same width (see fig. 3) and depth (layers interlaced with the phase change material,

which is written on having the same depth), therefor having intermediate conductive layers having same dimensions with the phase change material layers.

As for claim 11, Chen discloses the phase change material layers are made of Ge.sub.2Sb.sub.2Te.sub.5 (col.4, l.52).

As for claim 12, Chen discloses the plurality of conductive layers are made of W, TiW, etc. (col.4, l.44).

As for claim 13, Chen demonstrates the number of phase change material layers corresponds to the number of possible bit values storable (col.4, l. 36-38).

As for claim 22, Chen expresses memory technologies can be read only, write once only, or repeatedly read/write which represents a programming circuit that writes data to the array of multi-bit phase change memory cells; and a sensing circuit that reads out data from the array of multi-bit phase change memory cells. All other limitations of claim 22 are discussed above.

As for claim 23, see discussion to claim 11.

With respect to newly added claims 26-29, all limitations have been previously presented, and therefor are discussed in the rejection above.

Claim Rejections - 35 USC § 103

Claims 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Lowrey, in view of Klersy et al. of USPN 5,536,947.

Chen fails to demonstrate the plurality of phase change material layers are of similar resistivity (as in applicants' claim 3), and are made of the same or different material (as in claims 9 and 10).

Klersy et al. teaches compositional modification of phase change materials, including use of any means to modifying the compositions, such as modifying: the volume to yield stable values of resistance, which points to the plurality of phase change material layers having different dimensions (as in applicants' claim 6); and the phase change material layers made of the same or different material, as in claims 9 and 10 (col.14, l.3-54).

Claim Rejections - 35 USC § 103

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Lowrey, as discussed above, in view of Ovshinsky et al. of US 2004/0178401.

Chen fails to teach, the limitation to structure as recited in claim 8.

Ovshinsky illustrates all the limitations of claim 8 in figure 3, and explained in Example 1: a dielectric layer (60) formed between the first outer electrode (90) and the second outer electrode (30) and along sides of at least one other conductive layer (70) and a phase change material layer (80) disposed directly adjacent to the at least one other conductive layer (110).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of multi-bit phase changing memory device, of Chen, to include the structure of forming said device, as Ovshinsky, because

Ovshinsky demonstrates a specific structure exhibits the ability to modulate the threshold voltage between two electrodes of a multi-terminal device by applying a control voltage to a control terminal. This modulation effect represents improved functionality because the structure includes multi-terminal devices, a process improvement to the standard two-terminal devices.

Response to Arguments

Applicants assert, on page 8, that the reference of Klersy is not properly combined with Chen because it does not teach or suggest a muti-bit phase change memory cell (claim 1) or a multi-bit phase change memory (claim 22) wherein each of the phase change material layers have the same resistivity. Klersy teaches a multi-bit single cell memory (i.e. multi-bit memory cell) (see title) and a detailed description of how they function by phase changing (see background and col. 10, lines 15-25), including how a single cell can have multiple bits (see col. 1, line 42 and col.23, line 43), and the switching (i.e. the changing) of the phase material from the amorphous to the crystalline state, which is written on wherein each of the phase change material layers have the same resistivity (see col. 4, lines 41-53).

As to applicants assertion, on pages 8-9, even if the multiple layers of the volume of memory material in Klersy indeed formed of the same alloy, this fact alone may not be dispostive of whether these layers will have-the same resistivity, please see examiners annotation on Chen's teaching above, to provides specific details how the change of phase as in amorphous to the crystalline state or visa versa is written on

each of the phase change material layers have the same resistivity, also see response in the paragraph above which points to Klersy's teaching. It would have been very obvious to one of ordinary skill in the art at the time of invention was made, that a change to the states of the phase change material, as in Kersey or Chen, would indicated the materials having the same resistivity, as applicant's claimed limitation, because it is well known that memory devices are programmed between a generally amorphous state that exhibits a relatively high resistivity, and a generally crystalline state that exhibits a relatively low resistivity and that there are frequent times when the bits of the same cell are in the same state, having the same resistivity either programmed all "1" or all "0".

As to applicants remark, on page 10, that the reference of Chen intermediate conductive layers has a greater height and greater thickness than the height and thicknesses of each of the phase change material layers, examiner agree. However, the reference of Chen clearly illustrates the intermediate conductive layers have the same width (see fig. 3) and teaches that the layers are interlaced with the phase change material, which is written on having the same depth, therefor the intermediate conductive layers have same dimensions with the phase change material layers.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Patricia A George
Examiner
Art Unit 1765

PAG
03/07

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER